SPECIFICATION

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INTEGRATED CIRCUITS WITH PARALLEL SELF-TESTING

Cross Reference to Related Applications

This is a continuation-in-part of patent applications, titled: "Dual-Port Memory Cell", now U.S. PAT 6,552,951 USSN 09/806,299 ~~(attorney docket number: 98P 02816WOUS)~~ and "Memory Architecture with Refresh and Sense Amplifiers", USSN 10/131,364 ~~(attorney docket number: 00P 19334US01)~~ now U.S. PAT 6,628,541

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Background of Invention

[0001] Integrated circuits (ICs) such as digital signal processors (DSPs) include on-chip memory for storage of information. The on-chip memory typically comprises, for example, an array of memory cells connected by word lines in one direction and bit lines in another direction. The memory cells are routinely tested to ensure that the memory is properly readable or writable. Testing may be carried out by writing test patterns into particular memory locations and reading the test patterns to verify that both the written and read-out test patterns are consistent. Those memory locations that produce inconsistent results may be repaired through the use of redundancy schemes, if available.

[0002] Built-in self-testing (BIST) circuits may be embedded into the IC to improve the speed and versatility of testing without external hardware. The BIST circuit addresses, writes the test pattern and reads one memory location at a time. However, as the size of the memory increases, especially in multi-bank memory architectures, the number of memory locations to be tested will also increase. This requires more time to test the memory. The longer test times translate into higher manufacturing costs.

[0003] As evidenced from the above discussion, it is desirable to provide an improved